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CONVOLUTIONAL CHANNEL ENCODER/DECODER Final
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FINAL REPORT
FOR A
HIGH BIT RATE CONVOLUTIONAL CHANNEL
ENCODER/DECODER

June 20, 1977



LINKABIT CORPORATION
10453 Roselle Street
San Diego, CA 92121

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FOR A
HIGH BIT RATE CONVOLUTIONAL CHANNEL
ENCODER/DECODER

June 20, 1977

APPROVAL:

James W. Wilson
Contracting Officer
NATIONAL AERONAUTICS AND SPACE ADMINISTRATION
Lyndon B. Johnson Space Center
Houston, Texas 77058

LINKABIT CORPORATION
10453 Roselle Street
San Diego, CA 92121

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1.0 INTRODUCTION

This report is the final report of the development of a 50 MBPS Viterbi decoder system, developed under Contract No. NAS9-14936. Included in the system are the following major components:

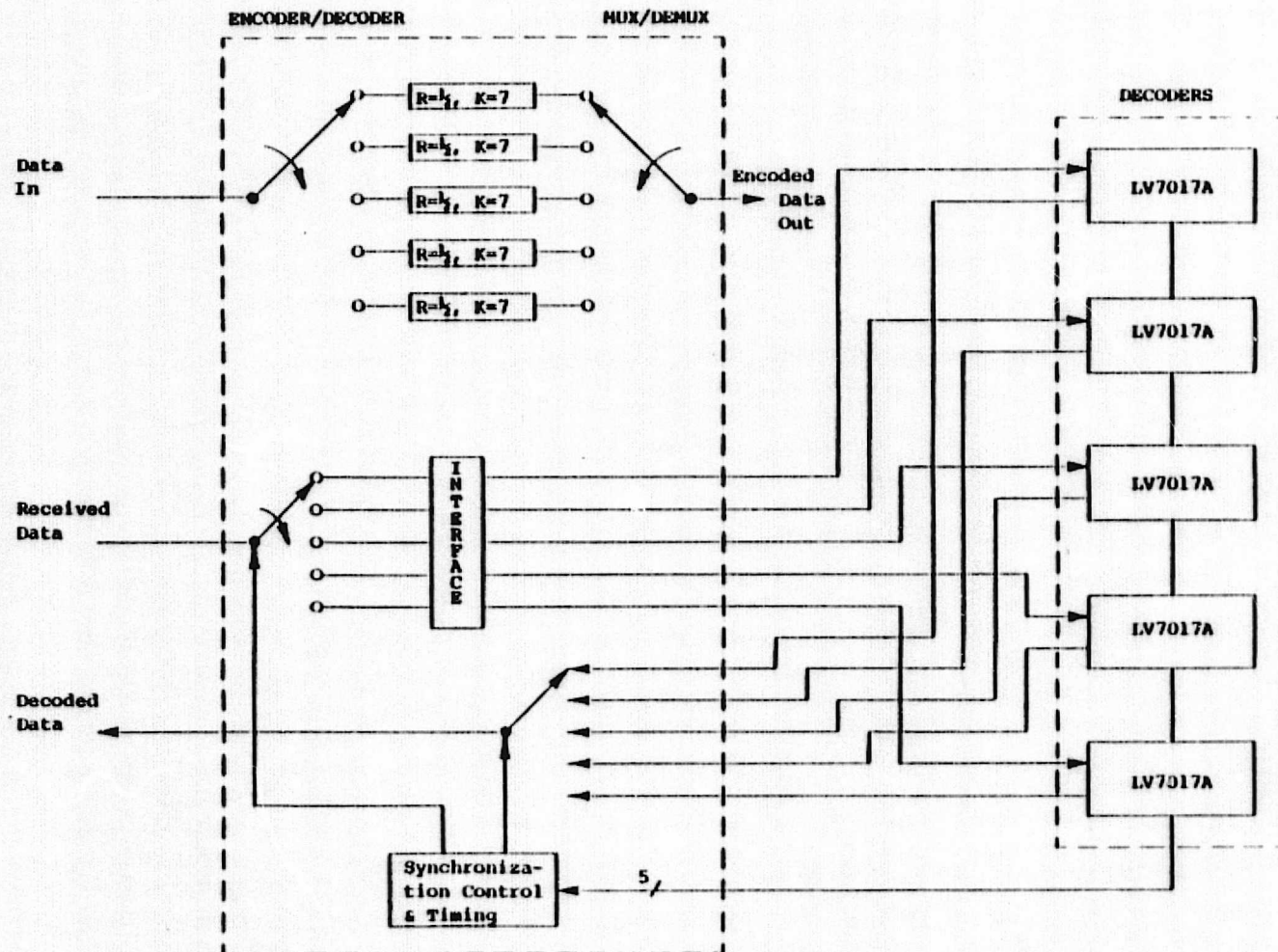
1. 50 MBPS encoder/decoder multiplexer/
demultiplexer
2. 50 MBPS data generator
3. 50 MBPS Convolutional Encoder
4. 50 MBPS error checker
5. 100 MBPS digital noise generator

This report will detail the design approach and trade-offs encountered during the development of the system, as well as problems encountered with the design of a high speed system and how they were resolved. Finally, a functional description of each of the major logical functions will be given. Section 5.0 contains the drawing package for the mux/test set portion of the system.

2.0 DESIGN APPROACH AND TRADE-OFFS

The LV7057 50 MBPS Viterbi decoder was implemented in two sections. The first section consists of five LV7017A 10 MBPS Convolutional encoder/Viterbi decoder systems. The second section consists of a single chassis containing a 50 MBPS Encoder and mux, a decoder mux/demux, synchronization circuitry, and test hardware. Figure 2.1 is a block diagram of the system, not including test equipment, showing its two major sections and some internal detail.

Figure 2.1 - System Block Diagram



2.1 ENCODER

Serial data at any rate from DC to 50 MBPS is input to the encoder demultiplexer where it is distributed to one of 5 rate 1/2, constraint length 7 encoders. Each of the encoders, operating at 1/5 of the data rate, generates two symbols. The symbols are then recombined to form a 100 MHz symbol stream. The order in which the coded symbols are recombined has a direct impact on the complexity of the decoder demultiplexer. If G_{ij} is the coded symbol due to the i -th generator of the j -th encoder, the symbols are recombined as follows:

$$G_{00}, G_{01}, G_{02}, G_{03}, G_{04}, G_{10}, G_{11}, G_{12}, G_{13}, G_{14}$$

Thus the symbols from a particular encoder are separated from each other by 4 symbols. This presents the decoder demultiplexer, which has no knowledge of the encoder timing, with a 1 in 10 ambiguity to resolve. Another recombination method, namely:

$$G_{00}, G_{10}, G_{01}, G_{11}, G_{02}, G_{12}, G_{03}, G_{13}, G_{04}, G_{14}$$

presents the decoder demux with only a 1 in 2 ambiguity. In the case of the LV7057, the former approach was taken due to customer preference. Had the latter approach been taken, significant savings could have been realized in terms of simplified synchronization circuitry and better sync recovery performance.

The sync information returned from the decoders is a function of the signal-to-noise ratio of the received data; that is, the decoder will assume it is in sync until it appears that the input signal-to-noise (E_b/N_o) drops below a certain fixed level. In the case of the LV7017A, this level is 2.5 dB. When the LV7017A has detected an apparent E_b/N_o less than 2.5 dB, a decision is made to change sync state, that is, when the demultiplexer is synchronized, the probability of a loss-of-sync false alarm is determined solely by the channel E_b/N_o . When the decoder demux is in an incorrect state, those decoders receiving incorrect symbols will appear to be receiving data with a very low signal-to-noise ratio, and thus will change sync with high probability. Information about which decoders are losing sync and which are not is used to determine the timing change needed to reach correct framing. A more detailed discussion of the methods involved will be included in the functional description of the sync circuit. Performance of the K=7, Rate 1/2 Viterbi decoder system in the presence of additive white Gaussian noise is shown in Figure 2.2.

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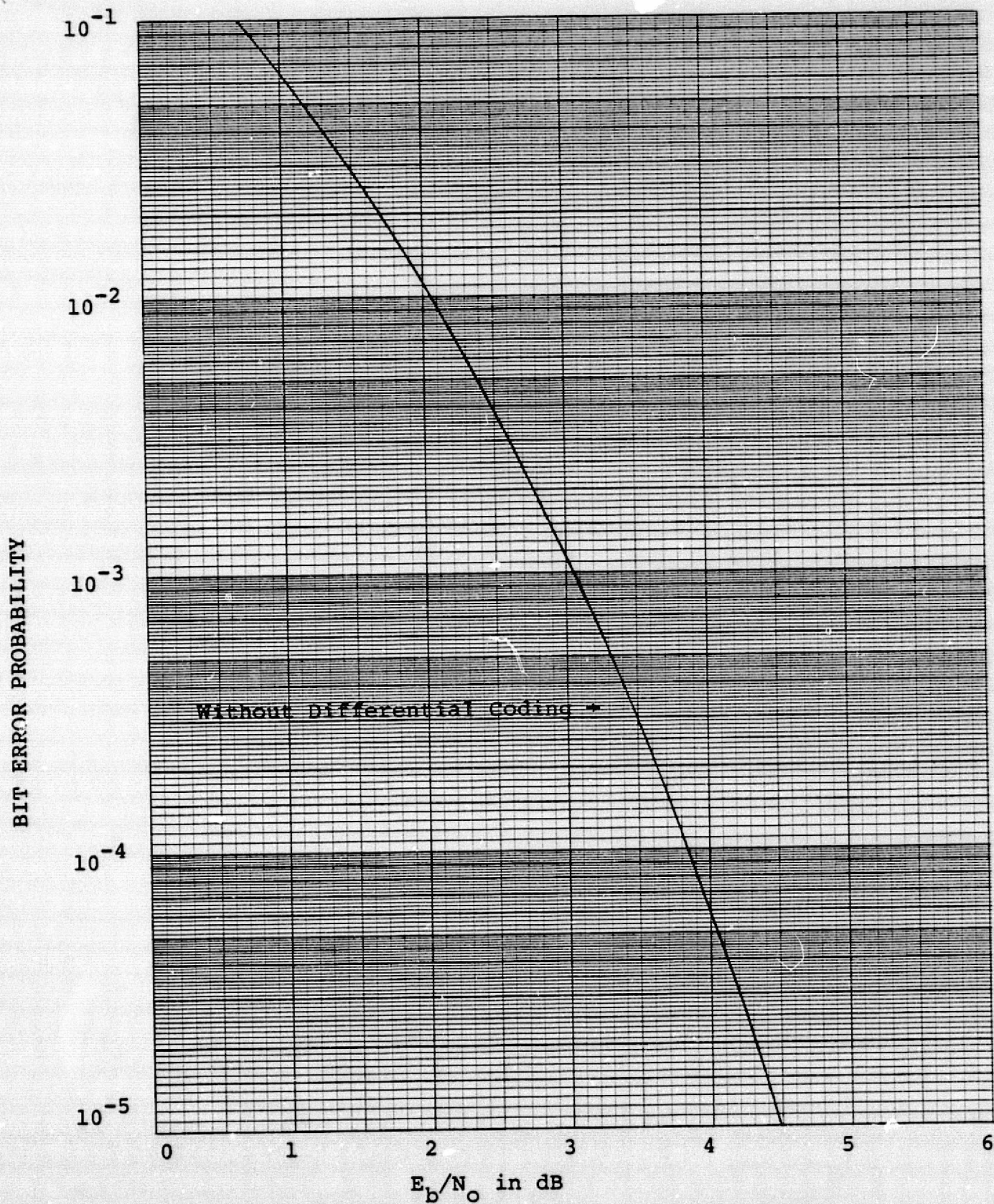


Figure 2.2 - Performance curve for the LV7057

2.3 DATA GENERATORS

The LV7057 Viterbi decoder system contains all of the test equipment needed to provide a complete end-to-end model of a coded communications system. Included in the test equipment are two data generators used to provide a data source. The first data generator simply repeats the state of a 16 position switch register on the front panel. The second generator is a pseudo-random sequence generator of a degree 15, in particular $x^{15} + x^{14} + 1$. Provision has also been made to allow the input of data from an external source.

2.4 DIGITAL SIGNAL SIMULATOR

To simulate wideband gaussian noise, a 100 MBPS noise generator has been implemented digitally in the LV7057 system. The noise generator is implemented as 4 identical noise generators, each operating at 25 MHz. A degree 52 pseudo-random sequence generator generates a 52-bit word at 25 MHz, 13 bits of which go to each of the 4 noise generators. For each level of noise desired, a read-only memory (ROM) must be provided to each of the 4 noise generators. The LV7057 contains 5 noise levels, 2,3,4,5, and 5.5 dB, thus the noise generator contains a total of 20 noise ROMs. The method used to generate noise in the LV7057 system is discussed in more detail in the functional description.

2.5 ERROR CHECKING

Data from either one of the internal data generators, or from an external source, is delayed by means of a RAM delay line and compared to the decoded data over a period of 10^6 , 10^7 or 10^8 bits, and displayed digitally on the front panel of the LV7057 system. A mode not available in the current system, but which should be considered for future implementation, would allow the accumulation of error data over an arbitrarily large time interval. This would allow measurement of arbitrarily small error rates.

2.6 RELIABILITY CONSIDERATIONS

During the design and implementation of the LV7057 Viterbi decoder system, two major design considerations which would alter system reliability became evident. The LV7057 is a very complex system containing over 1800 integrated circuits. Each of the LV7017A's has an MTBF of somewhat below 4000 hours. A militarized version of the same decoder, functionally identical except for reliability enhancements, has a computed MTBF of greater than 11,000 hours. When combined in a system such as the LV7057, the increase can make a dramatic difference in overall system reliability, while increasing the cost only a very little.

Another feature which could greatly increase system availability and reliability is the addition of a "roving" spare. This sixth decoder would be dynamically assigned by the decoder demux to the same slot that was currently being used by one of the 5 actual operating decoders. The mux then compares the outputs of the two decoders, and if they are the same, rotates the "spare" to another slot. If a discrepancy is encountered, the mux decides which unit, the spare or the active decoder, is at fault. If the active decoder is at fault, the spare is automatically swapped in and operation continues without manual intervention. A front panel indication is given so that the failed decoder may be repaired when it is convenient. Since this is a fully multiplexed system, the implementation of this feature would take place completely inside the multiplexer and would not affect the decoders at all.

3.0 PROBLEM AREAS

Problems encountered during the design and implementation of the LV7057 Viterbi decoder system fall into three categories; general problems associated with a high-speed prototype design; speed versus complexity problems; and interfacing problems. The following sections will deal with each of these areas.

3.1 GENERAL PROBLEMS

Designing a high-speed system using the ECL family of digital logic places much more emphasis on the design considerations of layout and termination than in slower speed designs. Because this system was to be implemented as a brassboard, we decided to use a welded wire technique for implementing circuit card assemblies. The ECL-10000 family of logic circuitry was chosen to implement the LV7057 because it would function well in a prototype environment and its speed was adequate. Each board was carefully laid out according to signal flow and signal entry and exit points. Resistor networks used to provide pull down voltage for the ECL logic were scattered in areas where they would be needed. The only real problem in this area of the design was the interpretation of vendor specifications for integrated circuits. A careful reading of the specifications of a 200 MHz universal shift register will reveal that if the circuit is to do any useful work at all, it cannot be operated above 75 MHz. Often such necessary numbers as minimum hold-time are not specified, as in the case of the MC12012, thus making design verification a difficult task. Fortunately, there were no occurrences of problems such as this that could not be designed around. In one case, in the synchronization circuitry for the decoder demultiplexer, a radical departure from the original circuit was required; removal of a counter and a shift register and the substitution of a prescaler. The change resulted in much higher reliability performance.

3.2 SPEED VERSUS COMPLEXITY

The implementation of the LV7057 required that some very complex functions, for example a digital noise generator, be implemented at very high speed. In the case of the noise generator, digital noise at 5 different levels is provided at the 100 MHz symbol rate. The noise generator function is performed by means of a table look-up method and so requires an access to a read-only memory. This implementation problem was solved by constructing 4 noise generators and generating 4 noise symbols in parallel, then remultiplexing the symbols back to 100 MHz. A similar approach was taken in the error checking circuitry. To provide digital delay between the source data and decoded data, a random access memory (RAM) delay line was used. Because of the excessive write cycle required with a typical RAM, it was necessary to check 4 bits at a time in parallel.

3.3 INTERFACING

During the design phase of the LV7057, many different approaches to the interfacing problem were explored. Because access to all circuit cards is by means of a swing-down front panel, and because all system interconnect is on the front panel, a means of connecting each of the circuit card assemblies (CCA's) to the front panel had to be found. Coaxial cable was rejected because of its bulk and because of the large number of them which would be required. Flat cable with single ended signals was rejected after experiments showed that cross-talk would exceed system noise margins. The final design was implemented with flat cables composed of twisted pairs. Each signal transmitted to the front panel is transmitted as a two sided signal and received with a differential receiver. This method provides controlled impedance connections between the front panel and the CCA's and preserves the system noise margin. Connections between subassemblies that are made on the front panel, for example, between the data source and the encoder subsystem, are made by means of a shielded twisted pair cable. Care must be taken that associated signals, for example, a clock and its associated data, are interconnected with cables that are very close to the same length.

4.0 FUNCTIONAL DESCRIPTION

This section will provide a complete detailed functional description of each of the CCA's in the LV7057 Viterbi decoder system. Reference will be made throughout this section to the drawings contained in Section 5.0.

4.1 ENCODER/DECODER MULTIPLEXER (3001)

This CCA contains all circuitry necessary to generate a coded data stream at 100 MHz from a 50 MHz data source. A 100 MHz clock (2RCK IN) is received from the modem via differential receiver U83 (see page 6 of LD3001). This clock is then divided by 2 to produce a 50 MHz clock (RCK) used to clock the data source. Uncoded data (DATA IN) is received via U83 and serial-to-parallel converted via U61 and U62. The 5 parallel data streams are then input to 5 identical rate $1/2$, constraint length 7, encoders. U63-U67 are shift registers through which each of the 5 data streams are shifted. For each bit shifted into the shift registers, two bits are output. The two bits are arranged in the order detailed in Section 2.1 and parallel-to-serial converted via shift registers U75-U77. The coded data and its associated clock are driven to the front panel by means of an ECL-3 gate (U81) with complementary outputs. Timing for the serial-to-parallel and parallel-to-serial converters is generated by the bi-quinary counter U78.

Soft quantized data is received into the decoder demultiplexer via differential receiver U1 (LD3001 page 1,2,3). Sheets 1-3 of LD3001 each contain functionally identical circuitry. A timing diagram for received data is given in Figure 4.1. Received data (SGN MSB, LSB) is serial-to-parallel converted into 10 bit words. These 10 words are then converted to TTL and then are output via current mode differential drivers (3453's) to LV7017A's. There are no frequency dependent

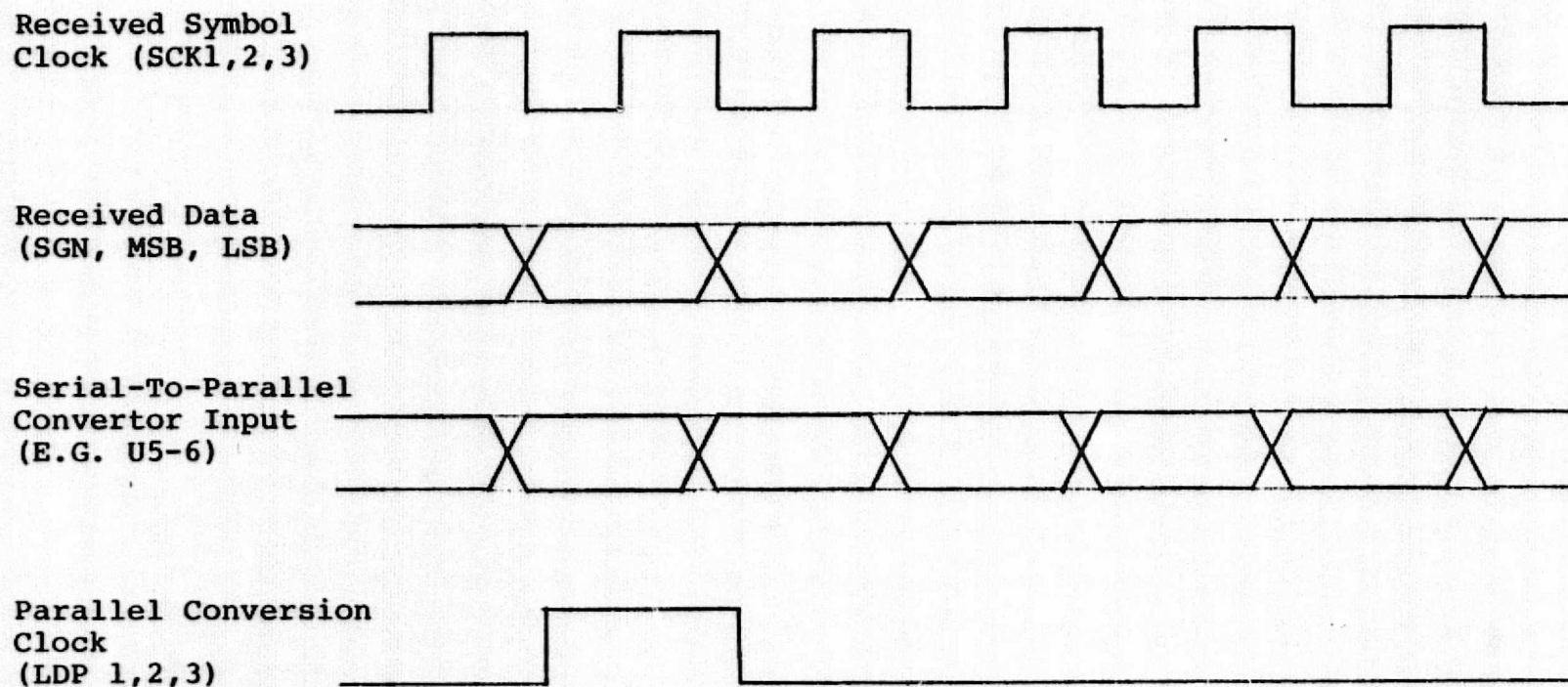


Figure 4.1 - Decoder Demux Input Timing

elements in the decoder demultiplexer circuitry. Delay associated with logical functions is independent of the clocking frequency, implying that circuit functionality at the highest allowable speed (100 MHz) ensures functionality at all lower speeds. As pointed out previously, the LV7017A's are operated as if they are receiving QPSK data and thus receive both symbols in parallel. Signal PDRCK is a 100 MHz clock which is transmitted to each of the decoders to provide data timing. Figure 4.2 illustrates symbol clock timing between the LV7057 and each of the LV7017A's.

Timing for the decoder demultiplexer is derived from the received symbol clock (2RCLK) which is received at U1 (page 4 of LD3001). The symbol clock is distributed via U56 to all other components of the demux. A prescaler (U57) nominally divides the symbol clock by 10 to provide the 10 MHz rate needed for the other elements. As mentioned previously, there is a potential 1-in-10 timing ambiguity in determining the appropriate symbols for each decoder. A signal from each decoder (SYNC1 through SYNC5) is used to determine whether the system is synchronized, and if it is not, what timing adjustments need to be made to obtain synchronization. Counters U52, U53 and U54 represent a divide-by-256 circuit which divides the signal PRDCK1 (maximum 100 MHz) and controls the sampling of sync status. Every 2560 information bits (512 bits per decoder) a sample of the current state of the decoder sync lines is stored in

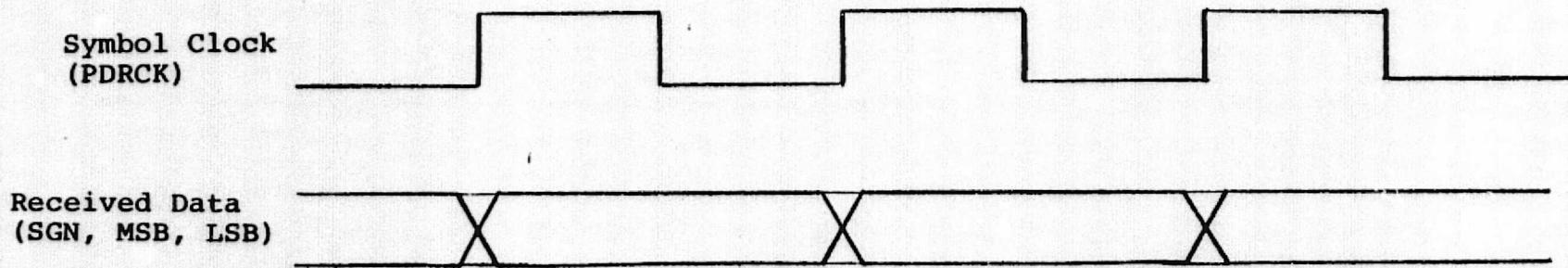


Figure 4.2 - Symbol Clock/Data Timing Relationship

latch U40. If the system is in synchronization, no action is taken. If one or more decoders are out of sync, then this information is used to address a ROM (U42), whose output will be an hypothesis of the number of symbol times which must be slipped in order to obtain sync. A bias has been built in to prevent marginal signal-to-noise conditions from causing excessive false alarms. An output of the ROM (U42) indicates whether the system is out of sync. This output controls the counting of U55. If the system was previously in sync, then an out-of-sync indication must be present for two sample periods (5120 bits) before new timing will be tried. Pin 15 of U55 controls the sampling of flip-flop U43. When the out-of-sync conditions are met, U43-10 goes high and enables the re-sync process; U51 is loaded with the output of the ROM and begins to count at 10 MHz. Until U51 overflows, U48-3 is low and prescaler U57 performs a divide by 11 instead of the normal divide-by-10. Timing signals generated by the divided output of the prescaler (LDP1,2 and 3) are used to latch the appropriate 10-bit word in the decoder demultiplexer.

Decoded data from the 5 LV7017A's is received via U36 and U37, (LD3001, sheet 5) latched and then converted to ECL levels in U45 and U46. The 5-bit parallel word is then converted to serial and output to the front panel via U60.

4.2 NOISE GENERATOR (3002)

This circuit card contains circuitry to simulate the output of an 8-level soft-decision modem operating on a channel disturbed by white Gaussian noise. A rotary switch on the front panel allows the simulated channel signal-to-noise ratio (E_b/N_o) to be set at 2.0, 3.0, 4.0, 5.0, or 5.5dB. There is also a switch which allows the noise to be turned off completely.

The modem output is represented by a 3-bit signed magnitude number. The interval probabilities are given by the following:

$$P(I_j|1) = \frac{1}{\sqrt{\pi N_o}} \int_{I_j} \exp \left\{ -\frac{(x - \sqrt{E_b})^2}{N_o} \right\} dx$$

and

$$P(I_j|0) = \frac{1}{\sqrt{\pi N_o}} \int_{I_j} \exp \left\{ -\frac{(x + \sqrt{E_b})^2}{N_o} \right\} dx$$

Where $P(I_j|i)$ is the probability of the modem output being in the j -th interval given that an i was transmitted. Because of our choice of signed-magnitude to represent the intervals, the above probabilities have the property that

$$P(I_j|0) = P(I_j^*|1) \text{ for all } j \text{ where } I_j^* \text{ is the interval}$$

whose sign bit is the complement of I_j and whose magnitude bits are the same. For example:

$$P(000|0) = P(100|1).$$

Thus, it is sufficient to generate, for each desired E_b/N_0 , a set of 3-bit words with probabilities

$$P(I_j|0) \quad I_j = 011, 010, 001, 000, 100, 101, 110, 111.$$

The hardware implementation of the noise generator uses a table look-up method. Basically, a ROM contains the 3-bit words in quantities proportional to their probability. For example, if the ROM could contain 256 3-bit words, and $P(000) = .004$, then the symbol 000 would appear in the ROM 1 time. The same allocation is carried out for the remaining words, and the ROM is addressed by a PN sequence. Since a PN sequence generates values with uniform probability, the output of the ROM reflects the probability of occurrence of the various intervals, as represented by their 3-bit entries.

To increase the accuracy of the noise generator, a scheme is employed whereby 8 bits are coded into 3 by means of a priority encoder. These bits then have the following non-uniform probabilities of occurrence:

$$\frac{129}{256}, \quad \frac{64}{256}, \quad \frac{32}{256}, \quad \frac{16}{256}, \quad \frac{8}{256}, \quad \frac{4}{256}, \quad \frac{2}{256}, \quad \frac{1}{256}$$

The first element is slightly higher than would be expected so that the sum of the probabilities is 1. These 3 bits,

together with the 5 remaining uniformly distributed bits are used as the ROM address. The resulting noise generator has an accuracy of $\pm 2^{-13}$. Each value of E_b/N_0 requires an 256×3 bit ROM. Figure 4.3 shows a block diagram of a noise generator section.

As explained previously, the noise generator is implemented in 4 identical noise generators whose output is multiplexed to the 100 MHz symbol rate. Each of these noise generators requires 13 pseudo-noise bits to generate one symbol of noise. Because of this requirement, a degree 52 pseudo-noise sequence generator was implemented to provide a sufficient number of bits. To maintain independence between 13-bit words, the entire generator is shifted 52 bits at a time. Figure 4.4 shows a block diagram of how the sequence generator, $1+X^3+X^{52}$, was implemented. The input to each stage is the current value of that stage XOR'ed with the value to be shifted into that stage 52 bits later, as determined by the polynomial being implemented.

The actual hardware implementation is given in LD3002 in Section 5.0. U1-U9 are an implementation of the sequence generator diagrammed in Figure 4.4. The 100 MHz symbol clock (2RCK) is received in U17 (LD3002 sheet 3). It is then divided by 4 in U12 to provide timing for the sequence and noise generators. U10 and U11 detect an "all-zeros" startup and force a "one" into the sequence-generator. This is done by allowing counters U10 and U11 to count whenever a "zero" is present at the output of the sequence generator and load

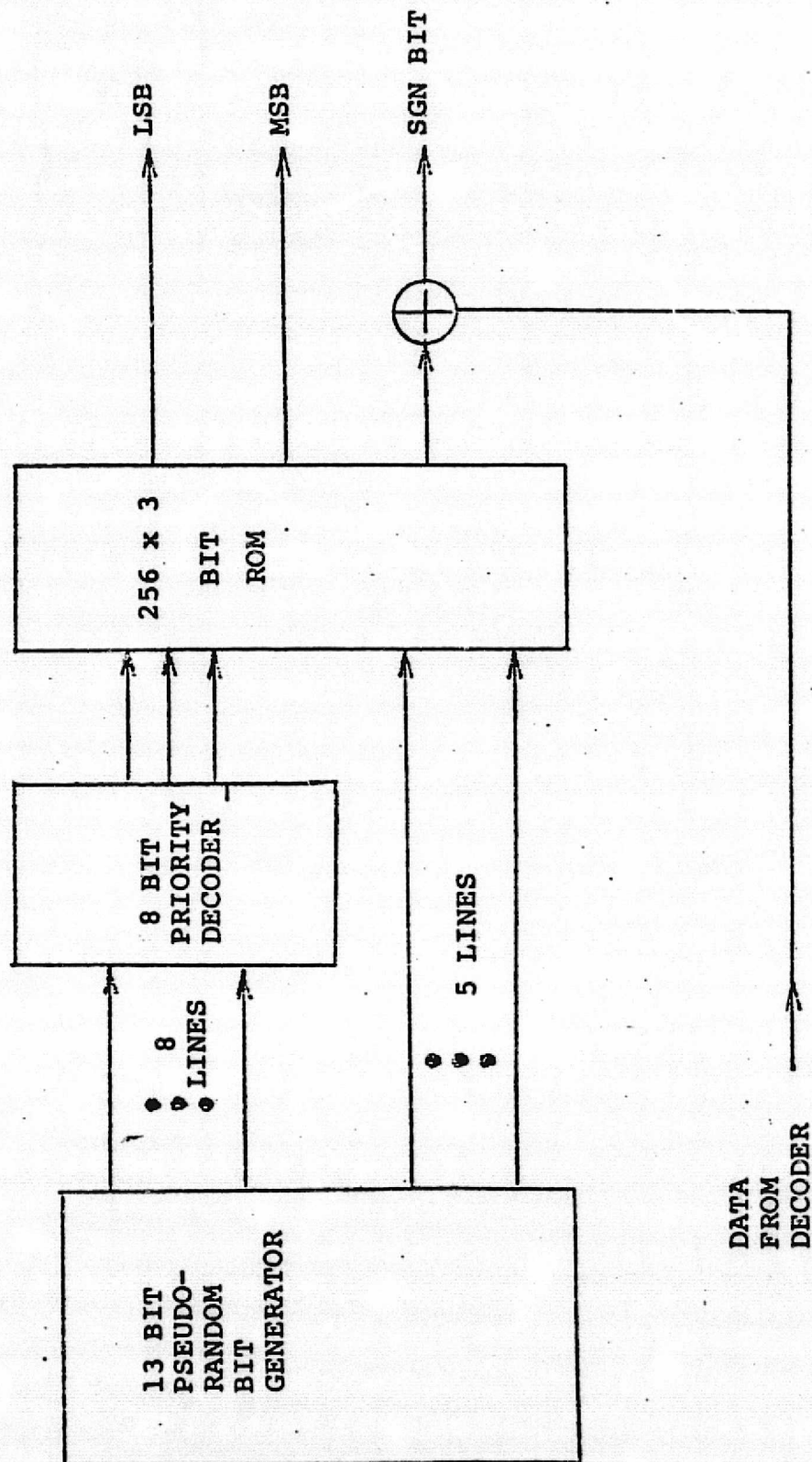
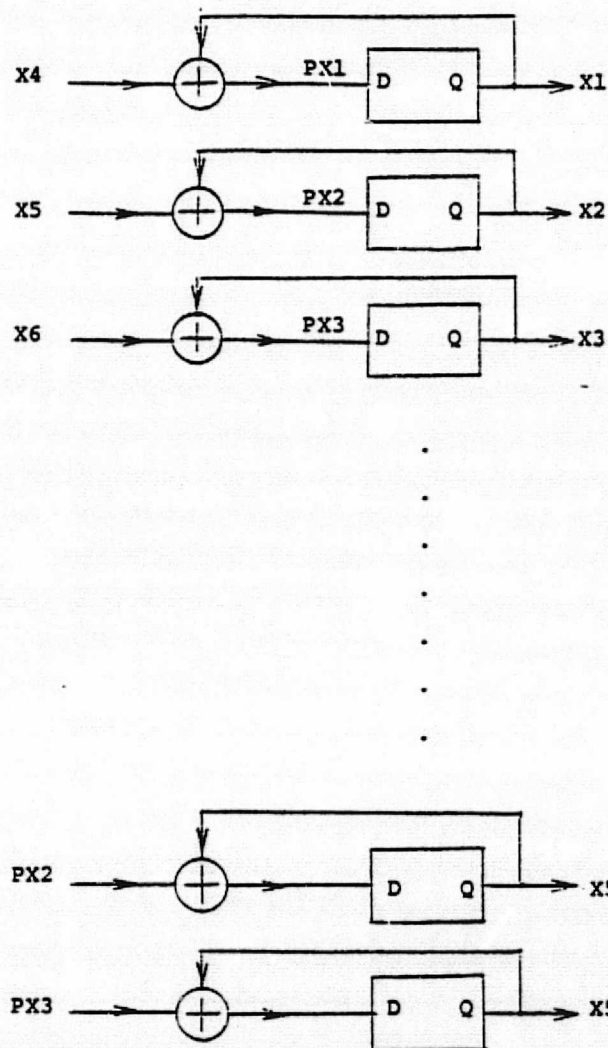


Figure 4.3 - A Digital Channel Simulator Functional Block Diagram



Machine state equivalent to serial implementation of $1+x^3+x^{52}$
 which shift 52 bits for every applied clock pulse.

Figure 4.4 - A 52-Bit Random Vector Generator

whenever a "one" is present. An overflow of the counter indicates that greater than 52 consecutive "zeros" have been generated and that the generator is "stuck". The overflow indicator is used to force a "one" into the sequence generator. Components U19-42 are four identical 25 MHz noise generators. Data from the input side of the sequence generator (PXn) is presented to the priority encoders, where it is latched and presented to the ROMs. The choice of stages to assign to particular latches and ROMs was made using circuit layout as the chief criteria. Noise selection is by means of signals SN1-SN5. The parallel symbols, H1-H12 are latched and become G1-G12 in U49 and U50. U14, U18 and U51 provide a means for measuring the interval probabilities actually generated for each of the 4 noise generators. TP15 and TP16 are used to select one of four generators, and a pulse is generated on TP1 and TP16 corresponding to the occurrence of symbols 000-111. The latched symbols G1-G12 are then converted to serial in U46-U48, combined with the noiseless coded data in U45, latched in U43 and U44, and driven to the front panel. Appendix 1 shows the output of a computer program used to generate the noise ROMs used in the noise generator detailed in this section. Included are computed symbol probabilities, approximated symbol probabilities, percentage error, and ROM truth table.

4.3 PATTERN GENERATOR - ERROR CHECKER (3003)

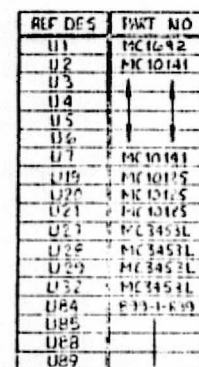
LD3003 in Section 5 gives a logic diagram of the pattern generator - error checker section of the LV7057 Viterbi decoder system. One of three sources for data may be chosen from the front panel; repeated data from a front panel 16-bit switch register; a degree 15 pseudo-noise sequence generator ($X^{15}+X^{14}+1$); or external data. Components U5-U8 form a 16-bit latch/shift register into which the switch register data is input when operating in that mode, or which forms the shift register for the sequence generator when operating in PN mode. The data rate clock (PRCK) is received in U1 and distributed. U2 is used as a mux to select which data source is to be used. U3 is used as a "zero detector" when the sequence generator is selected as the source. This prevents the generator from staying in the all-zeros state and provides a data synchronization pulse. The generated data is then driven to the front panel via U15.

A 100 MHz oscillator (U14) is provided for test purposes. The output of the oscillator is driven to the front panel via U15.

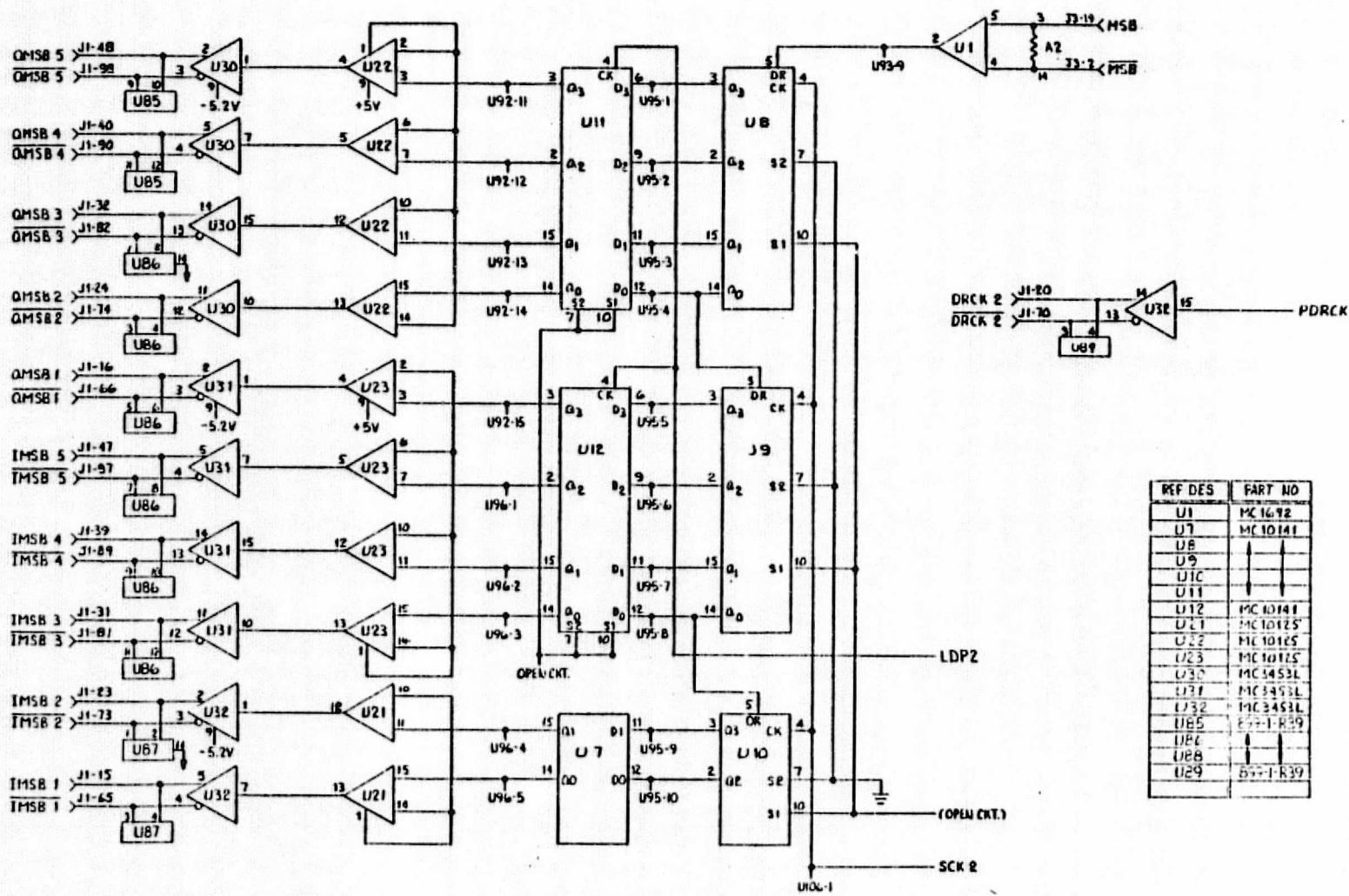
An error checking circuit is provided to detect discrepancies between the data source and the decoded data. Decoded data (DC DATA) and clock (D RCK) are received in U1, where the decoded data is converted to 4-bit words and then to TTL levels. Data from the 16-bit shift register U5-U8 is input to U19 (LD3003 sheet 3) where one of the eight lines

is selected. This circuit allows some variable delay (± 4 bits) between the data source and the decoded output. The delayed source data is then serial to 4-bit parallel converted (U50) and converted to TTL levels (U12). This source data is then input to a RAM delay line (U43 and U44) where it is delayed by an amount determined by the base address of the address generator (U37-U38). The output of the delay line is selected (U57), latched (U25), and compared to the decoded data. Errors are accumulated over periods of 10^6 , 10^7 , and 10^8 bits. The least-significant digit of the error display is stored in U22 and summed in U21, a ROM programmed to be a special purpose BCD adder. Whenever the least-significant digit overflows a signal (U21-9) is generated to increment the next front panel digit. Counters U28-U35 are the 10^6 , 10^7 and 10^8 , period generators, where timing is generated to update the front panel display every 10^6 , 10^7 or 10^8 bits. Components U39-U42 and U45 detect an error rate higher than 10^{-1} and force a change in the state of signals CQ1-CQ3, which in turn changes the absolute delay between the data source and decoded data (LD3003 sheet 3). The absolute delay may be varied ± 4 bits. The centering of this window is determined by the connections between signals X1-X15 (LD3003 sheet 1) and PSD1-PSD81 (U19 of LD3003 sheet 3).

5.0 LOGIC DIAGRAMS

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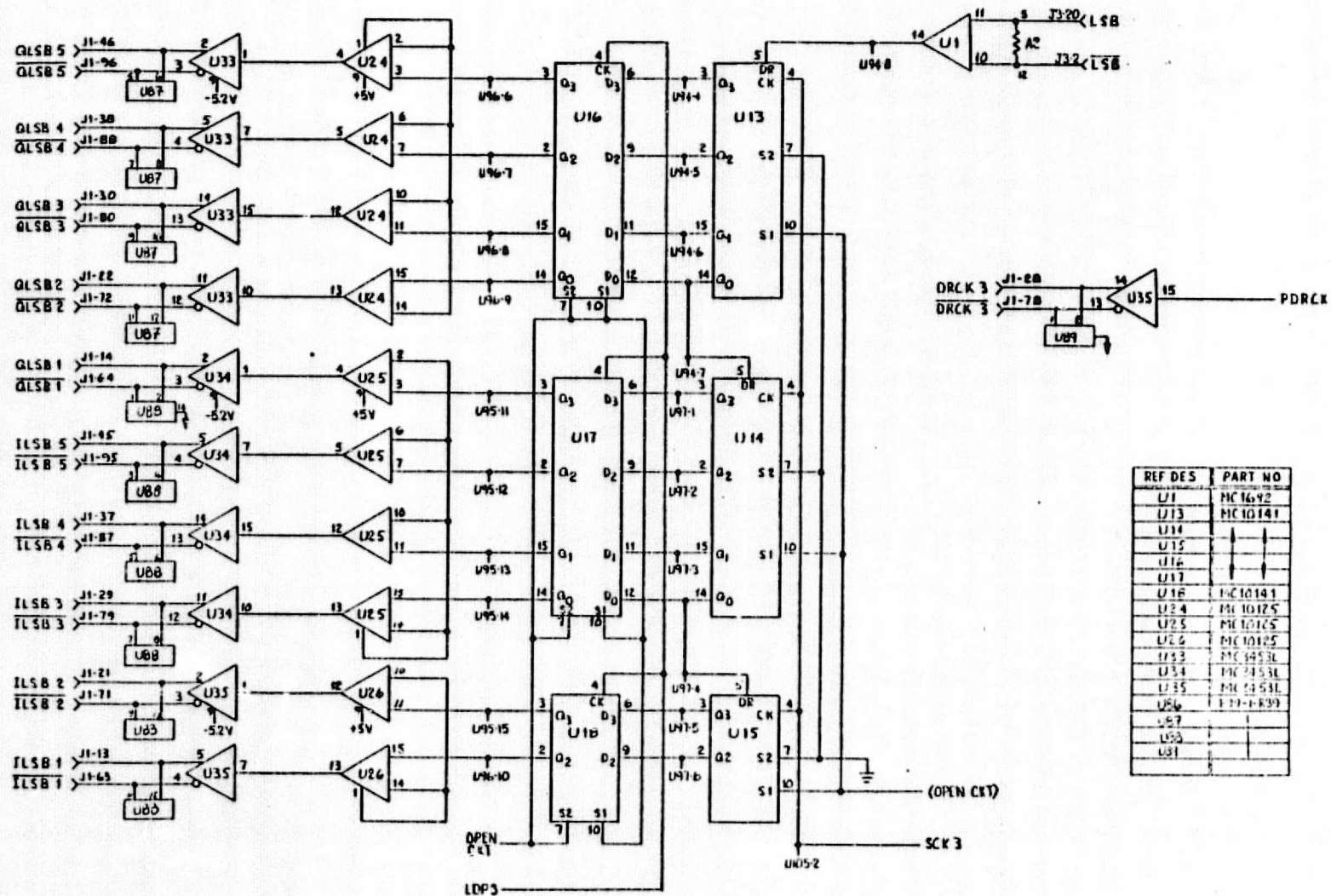
-33-



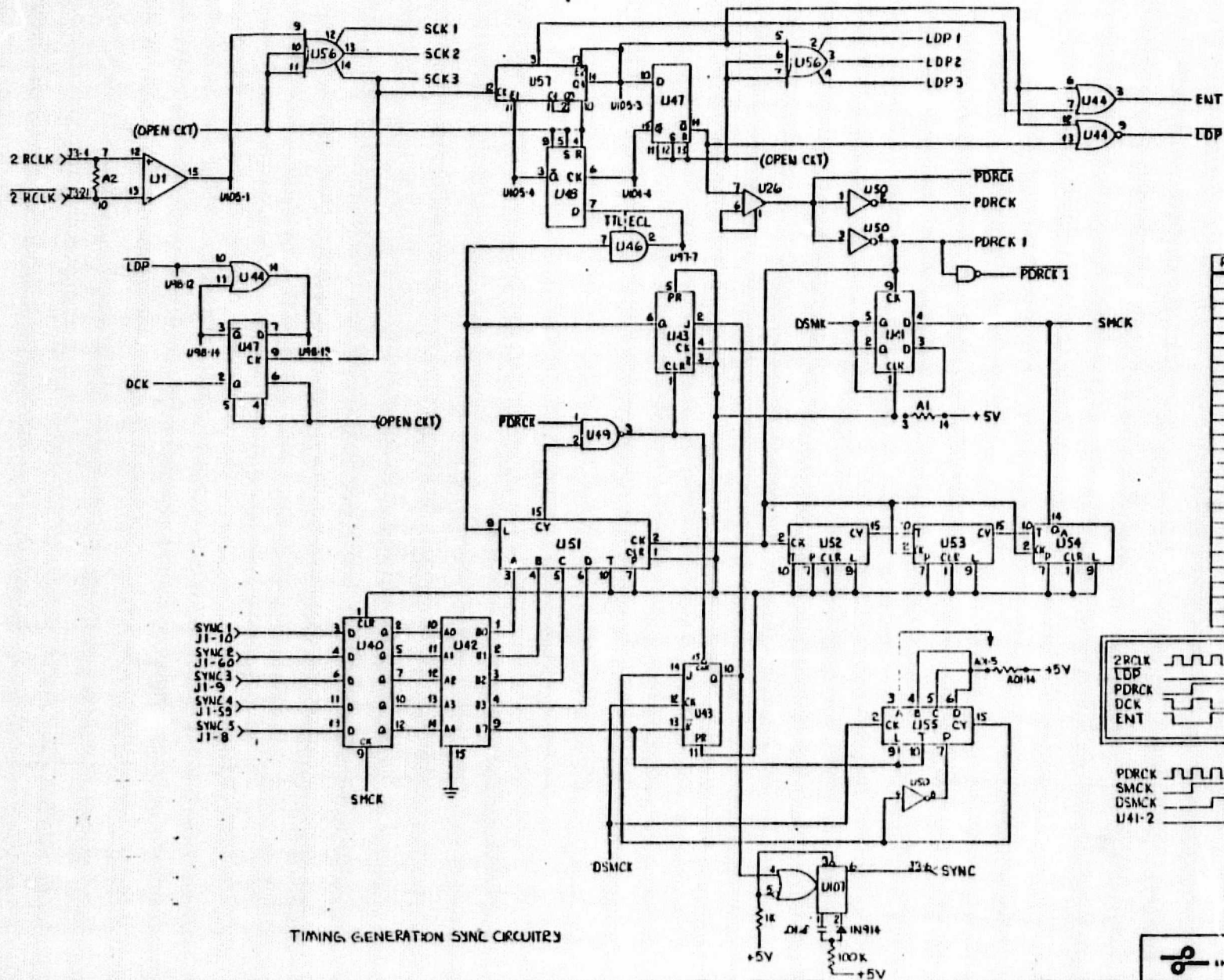
MSB SERIAL-TO-PARALLEL

8 7 6 5 4 3 2 1

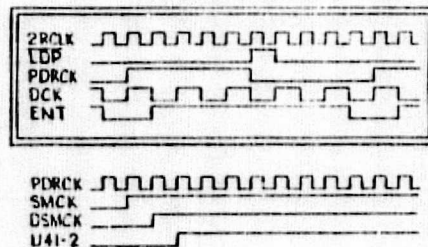
-34-



REF DES	PART NO
U1	MC 1642
U13	MC 10141
U14	
U15	
U16	
U17	
U18	MC 10141
U24	MC 10125
U25	MC 10125
U26	MC 10125
U33	MC 1453L
U34	MC 1453L
U35	MC 1453L
U36	111-1-K39
U37	
U38	
U39	



REF DES	PART NO	REF DES	PART NO
U1	MC1642	U57	MC1012
U26	MC10125		
		R4	10006165
		R5	10006165
U40	SN74LS174		
U41	SN74LS174		
U42	SN74LS123		
U43	SN74LS103		
U44	MC10103		
U46	MC10124		
U47	MC10131		
U48	MC10131		
U49	SN74LS00		
U50	SN74LS04		
U51	SN74LS163		
U52	SN74LS163		
U53	SN74LS163		
U54	SN74LS163		
U55	SN74LS163		
U56	MC10120		

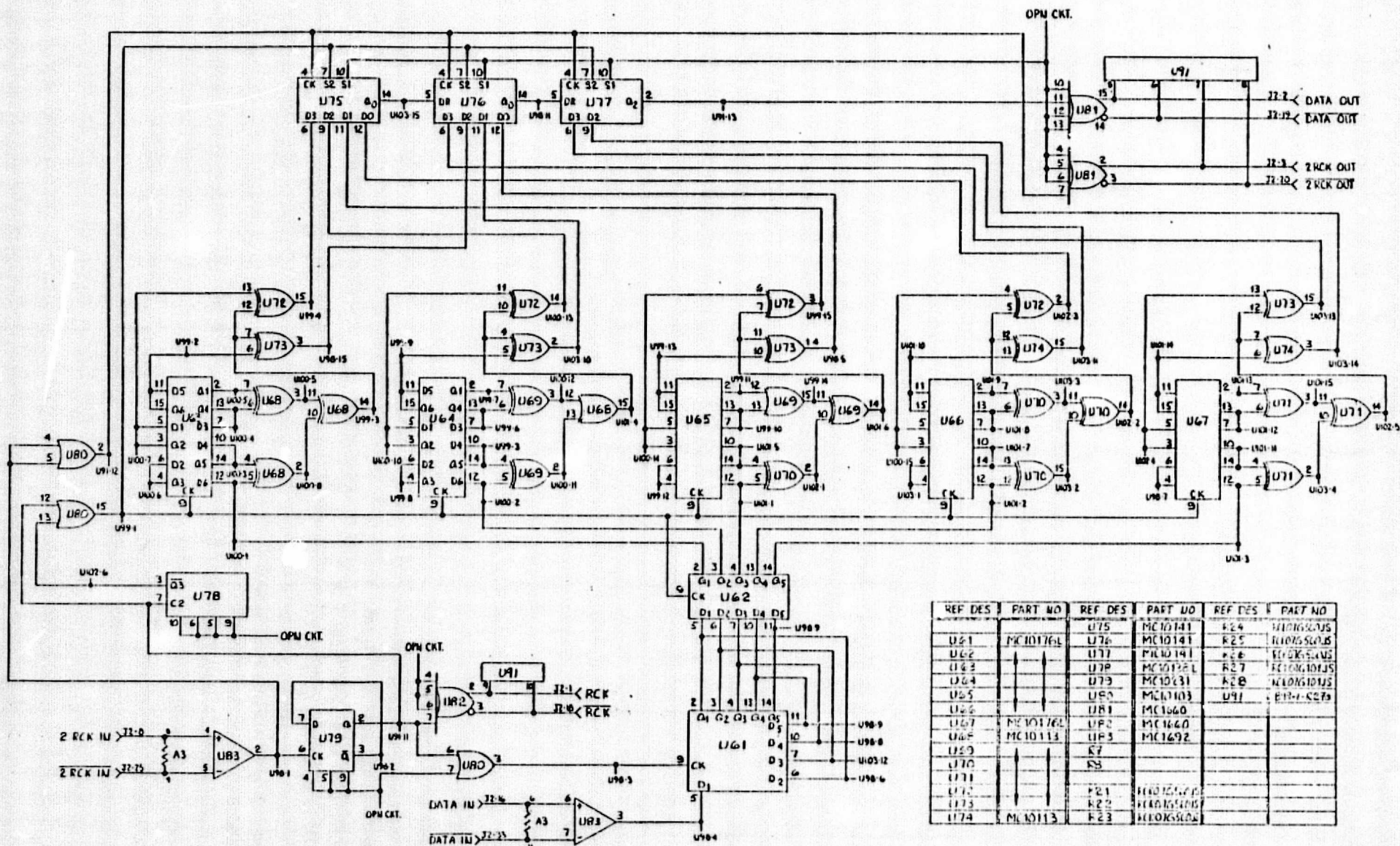


1987-1988 is shown in Table 1. The total number of birds was 1,000. The total number of birds was 1,000. The total number of birds was 1,000.



REF DES	PART NO	REF DES	PART NO
U7B	MC3450L	R7	NR06150
U37	MC3450L	R8	
U39	MC3450L	R9	
		R10	
		R11	
U44	MC10103	R12	
U45	MC10103	R13	
U46	MC10103	R14	
U5F	MC10141	R15	NR06150
U59	MC10141	R16	NR06150
U60	MC1660	R17	NR06150
U90	MC1660	R18	NR06150
U91	MC1660	R19	NR06150
		R20	NR06150
U6	NR06150		

DECODER OUTPUT PARALLEL-TO-SERIAL



REF DES	PART NO	REF DES	PART NO	REF DES	PART NO
U61	MC101764	U75	MC10141	R24	RL01650US
U62		U76	MC10141	R25	RL01650US
U63		U77	MC10141	R26	RL01650US
U64		U78	MC10151	R27	RL01650US
U65		U79	MC10131	R28	RL01650US
U66		U80	MC11103	U91	RL01650US
U67	MC101762	U81	MC10600		
U68	MC101113	U82	MC1660		
U69		U83	MC1692		
U70		K7			
U71		K8			
U72		R21	RL01650US		
U73		R22	RL01650US		
U74	ML101113	R23	RL01650US		

ENCODER

8

7

6

5

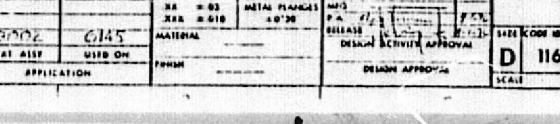
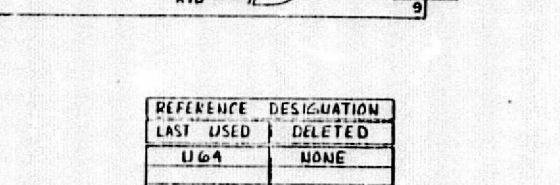
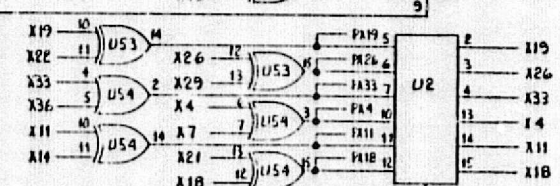
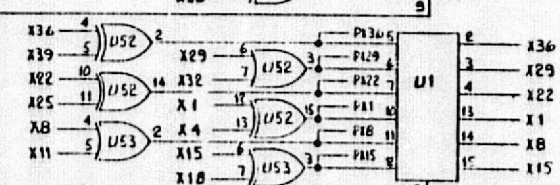
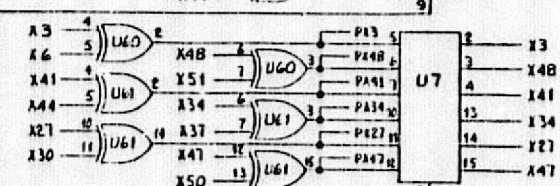
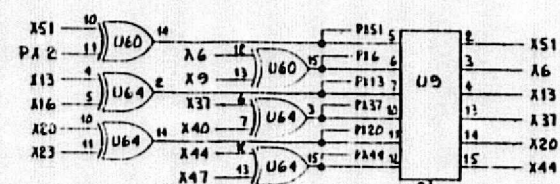
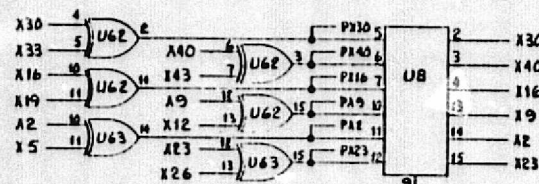
4

3

2

1

REV	DESCRIPTION	DATE	APPROVED
1004 112			



REF DES	PART NO
U1	MC10176
U2	
U3	
U4	
U5	
U6	
U7	
U8	
U9	MC10176
U10	MC10152
U11	MC10152
U12	MC10221
U13	MC10210
U45	MC10113
U52	MC10113
U53	
U54	
U55	
U56	
U57	
U58	
U59	
U60	
U61	
U62	
U63	
U64	MC10113

REFERENCE DESIGNATION	
LAST USED	DELETED
U64	NONE
R18	NONE

SEE SEPARATE PARTS LIST: PL

PSEUDO-NOISE SEQUENCE GENERATOR

2 REFERENCE DRAWING NO:
ASSEMBLY DRAWING 3002
PARTS LIST PL3002

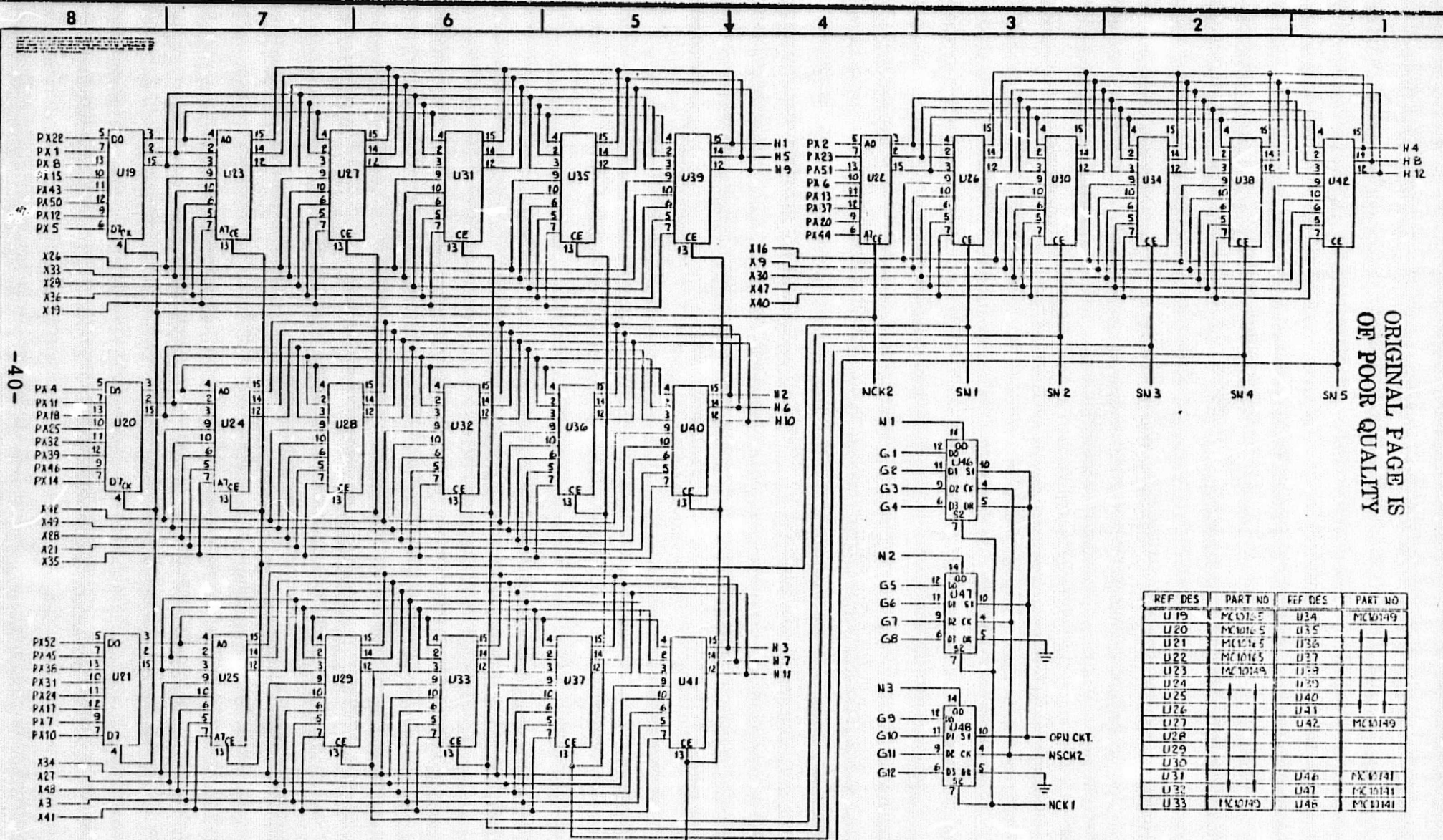
1 INTERPRET DRAWING PER MIL-STD-100 AND MIL-D-1000,
FORM 3 INTERPRET REF DES PER USA3 Y32.16.

NOTES: UNLESS OTHERWISE SPECIFIED

4 PARTIAL REFERENCE DESIGNATIONS ARE SHOWN FOR
COMPLETE DESIGNATION PREFIX WITH ---

3 ALL RESISTOR VALUES ARE IN OHMS

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND INCLUDE CREW APPLIC OR PLATED FINISHES		CONTRACT NO. N459-14936		TITLE NOISE GENERATOR	
DRAWN: []		DATE: []		REV: []	
CHECKED: []		DATE: []		REV: []	
APPROVED: []		DATE: []		REV: []	
MATERIAL: []		FINISH: []		SCALE: []	
APPLICATION: []		DESIGN APPROVAL: []		SIZE CODE IDENT NO: []	
NEXT ASSY: []		USED ON: []		D 11627	
PART NO: []		REV: []		L03002	
SHEET 1 OF 2					

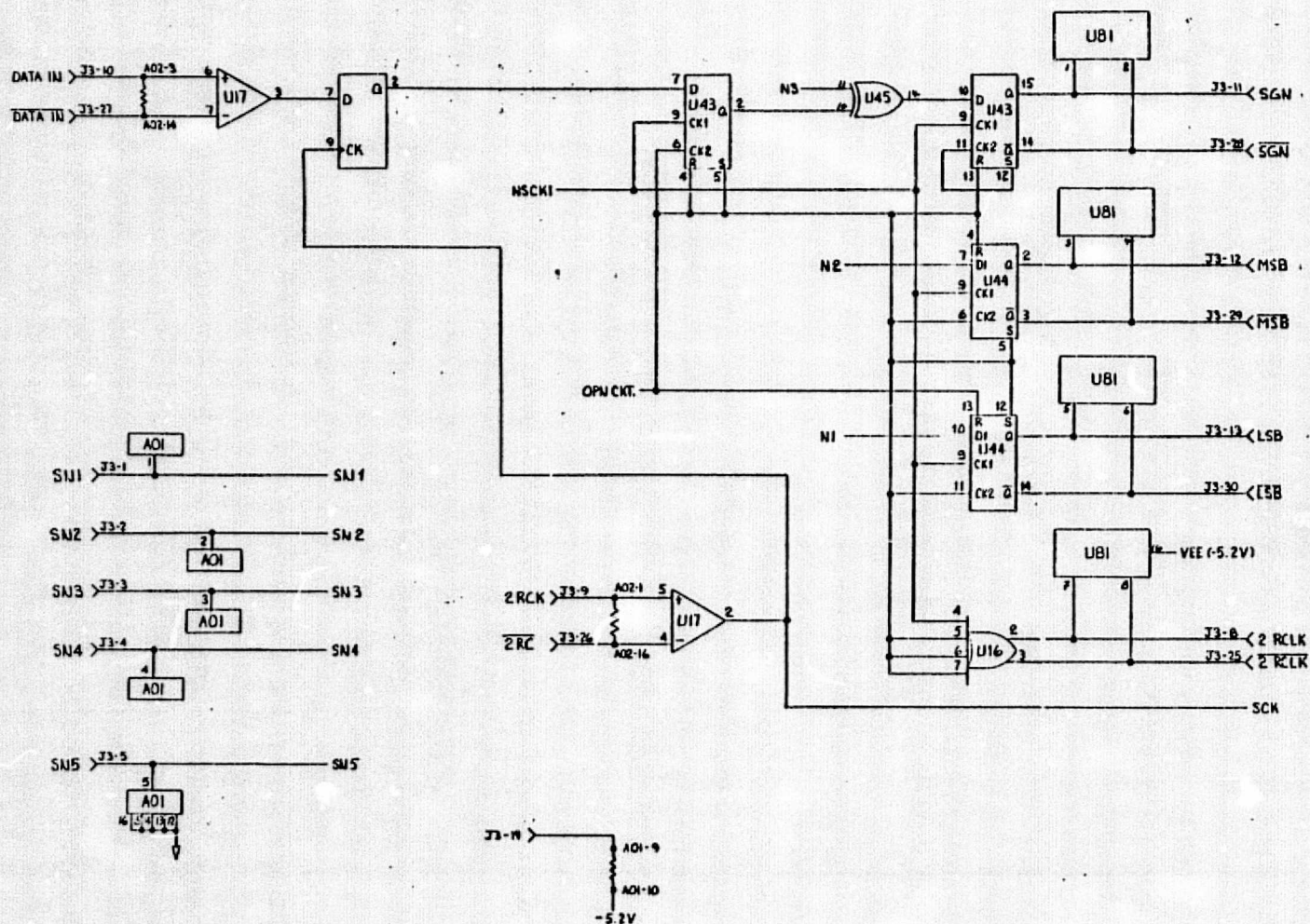


ORIGINAL PAGE IS
OF POOR QUALITY

REF DES	PART NO	REF DES	PART NO
U19	MC10145	U34	MC10149
U20	MC10145	U35	
U21	MC10145	U36	
U22	MC10145	U37	
U23	MC10149	U38	
U24		U39	
U25		U40	
U26		U41	
U27		U42	MC10149
U28			
U29			
U30			
U31		U46	FX10141
U32		U47	MC10141
U33	MC10149	U48	MC10141

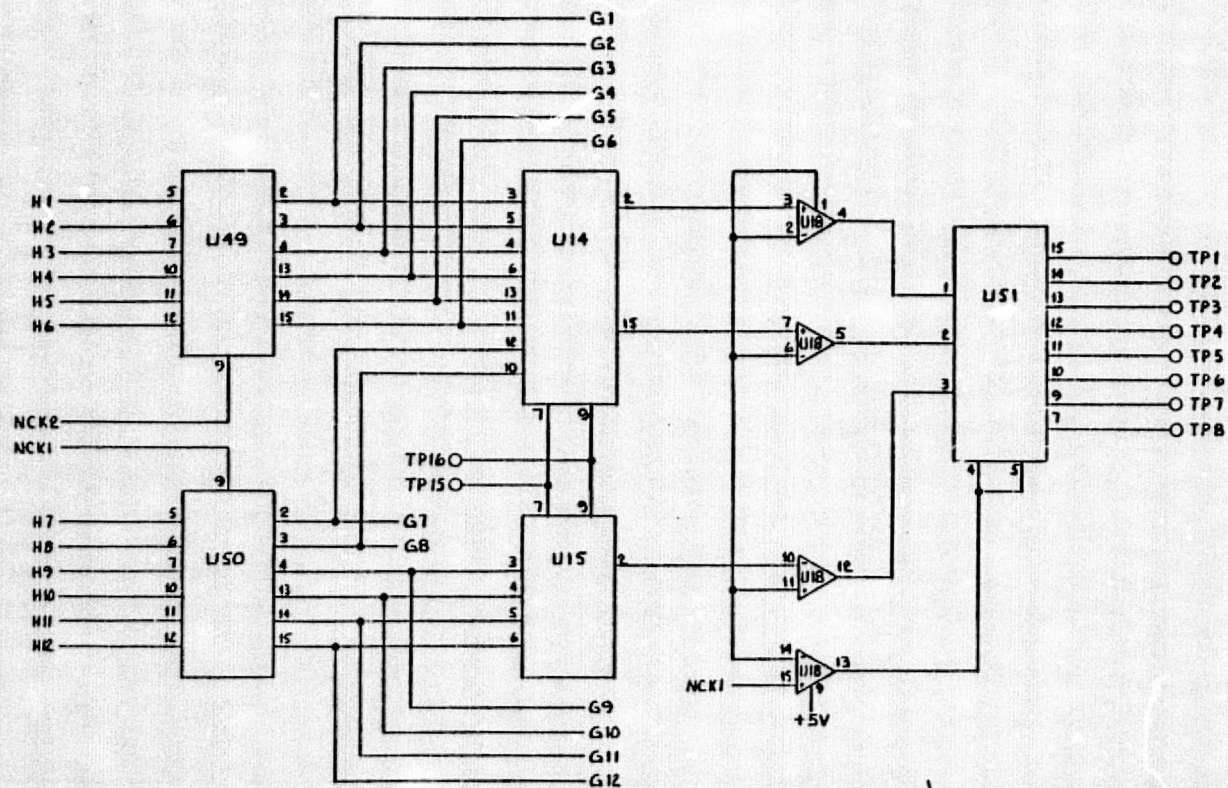
FOUR PARALLEL NOISE GENERATORS

ORIGINAL PAGE IS
OF POOR QUALITY



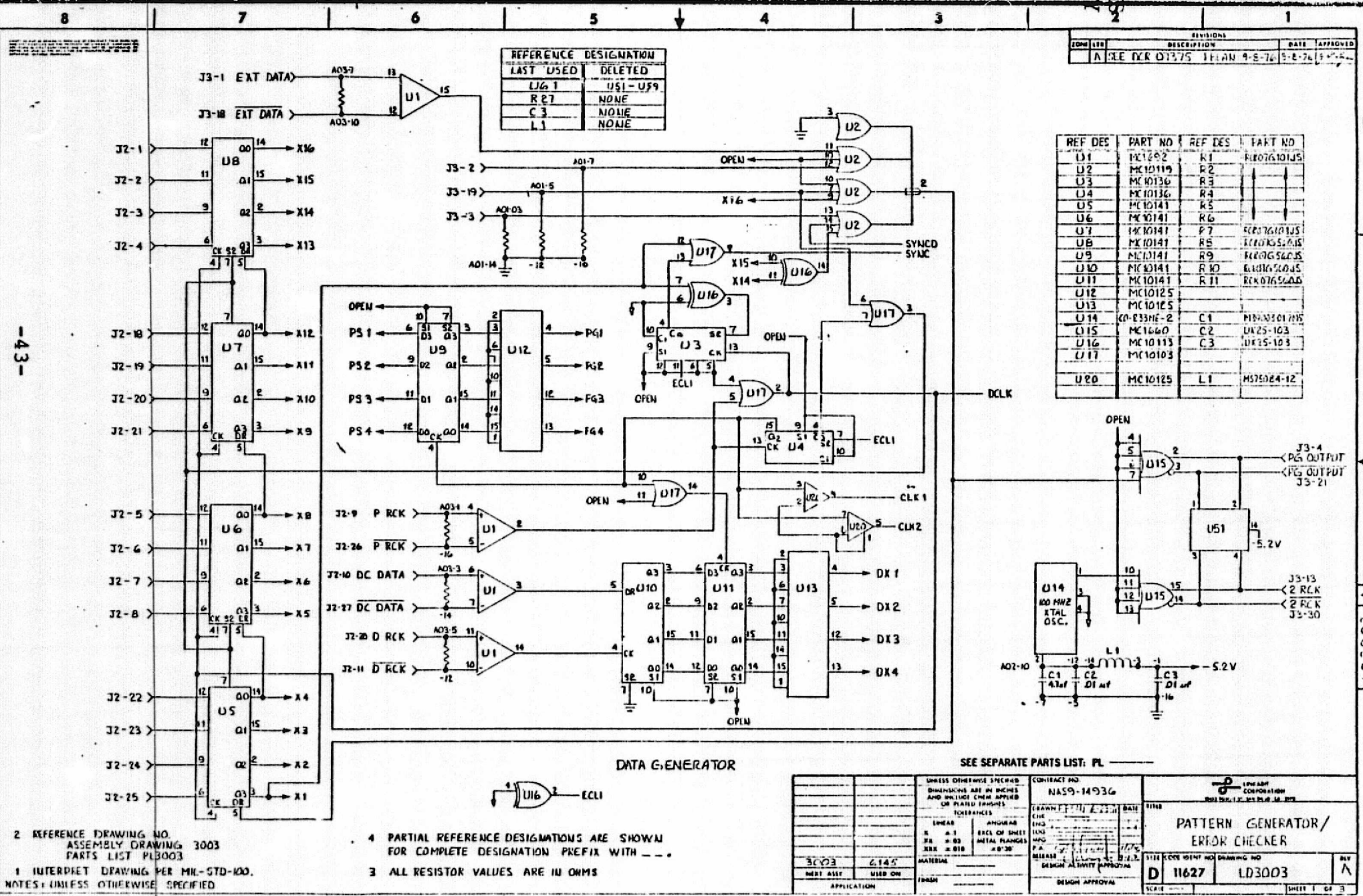
REF DES	PART NO
U16	MC1660
U17	MC1692
U43	MC10237
U44	MC10231
U45	MC10113
R1	R1076101J
R2	R1075560J
R3	
R4	
R5	R1026501J
R8	R1025560J
R9	
R10	
R11	R1076560J
R12	R1075101J
R13	
R14	
R15	
R16	
R17	R1076101J

NOISE MIXING/OUTPUT



REF DES	PART NO
U14	MC10174
U15	MC10174
U18	MC10125
U49	MC10174
U50	MC10174
U51	SN74S13B
R6	6K0XG101J5
R18	6K0XG101J5

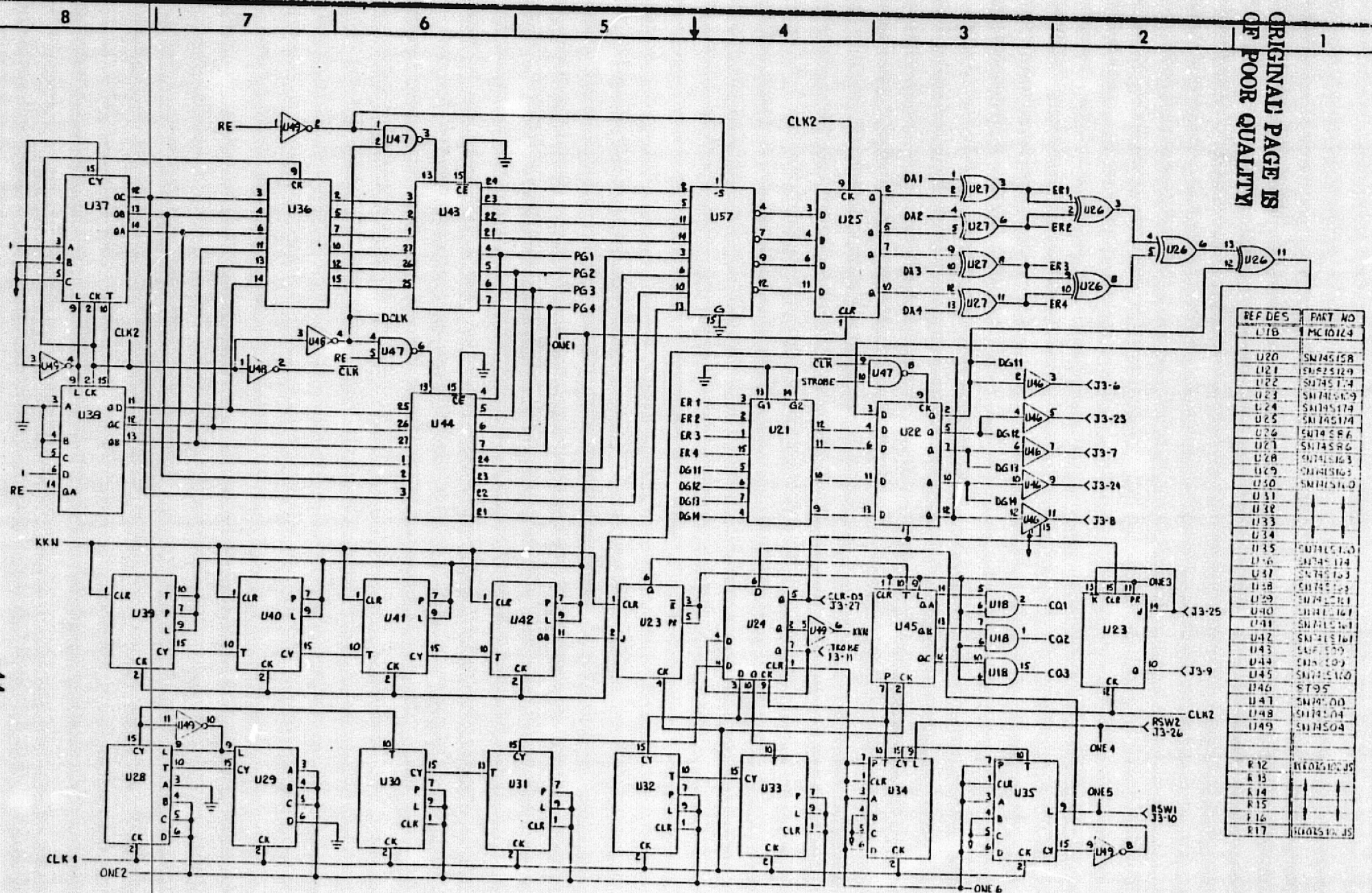
SYMBOL PROBABILITY MEASUREMENT



-43-

D
C
B
A
LD3003

ORIGINAL PAGE IS
OF POOR QUALITY

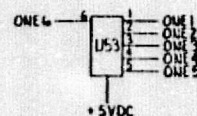


ERROR CHECKING/PERIOD GENERATION

REF DES	PART NO
U18	MC10124
U20	SN74S158
U21	SN74S129
U22	SN74S174
U23	SN74S169
U24	SN74S174
U25	SN74S174
U26	SN74S166
U27	SN74S166
U28	SN74S166
U29	SN74S166
U30	SN74S166
U31	
U32	
U33	
U34	
U35	SN74S166
U36	SN74S174
U37	SN74S166
U38	SN74S166
U39	SN74S166
U40	SN74S166
U41	SN74S166
U42	SN74S166
U43	SN74S166
U44	SN74S166
U45	SN74S166
U46	ST95
U47	SN74S166
U48	SN74S166
U49	SN74S166
R12	1K0051K JS
R13	
R14	
R15	
R16	
R17	1K0051K JS

11627 LD3003

-45-



VARIABLE DELAY GENERATOR
DECODER SYNC STATUS RECEIVERS

SIZE	CASE IDENT NO	LABORATORY NO
D	11627	LD3003

APPENDIX 1

Noise ROM Statistical Data

ORIGINAL PAGE IS
OF POOR QUALITY

RATE 1/2 THRESHOLD=0.500 ERN0= 2.000

INTERVAL PROBABILITIES ARE

P(111)=0.002899
P(110)=0.009044
P(101)=0.027351
P(100)=0.064733
P(000)=0.119919
P(001)=0.173697
P(010)=0.197405
P(011)=0.404748

	111	110	101	100	000	001	010	011
129-	0	0	1	4	7	11	9	0
64-	0	1	1	0	1	0	7	22
32-	0	0	0	0	0	0	0	32
16-	1	0	1	0	0	0	0	30
8-	0	1	1	1	1	0	0	28
4-	1	0	1	1	1	1	1	25
2-	1	1	1	1	1	1	0	26
1-	1	0	1	1	1	0	1	27

ACTUAL PROBABILITIES ARE

P(111)=0.002807
P(110)=0.009033
P(101)=0.027343
P(100)=0.064719
P(000)=0.119873
P(001)=0.173950
P(010)=0.197021
P(011)=0.405151

PERCENTAGE ERROR

-3.17%
-0.12%
-0.03%
-0.03%
-0.03%
-0.03%
-0.03%
0.09%

ORIGINAL PAGE IS
OF POOR QUALITY

LMCN-2.0 DB		NOISE ROM 2.0 DB		325129		(XXXXXX) JDB-		PAGE 1
OUTPUT FORMAT-H								
	0/8	***1/***9	***2/***A	***3/***B	***4/***C	***5/***D	***6/***E	***7/***F
000*	0001 0000	0002 0001	0007 0007	0003 0001	0002 0001	0003 0001	0003 0002	0003 0001
001*	0000 0000	0004 0006	0007 0007	0007 0007	0000 0004	0000 0004	0001 0000	0000 0000
002*	0000 0004	0006 0006	0007 0007	0007 0007	0007 0007	0005 0006	0004 0005	0006 0007
003*	0004 0004	0006 0006	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007
004*	0004 0004	0006 0006	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007
005*	0004 0004	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007
006*	0005 0005	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007
007*	0005 0005	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007
008*	0005 0005	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007
009*	0005 0005	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007
00A*	0005 0005	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007

ORIGINAL PAGE IS
OF POOR QUALITY

LMCN-2.0 DB		NOISE ROM 2.0 DB		625129		(XXXXXX) JOB-		PAGE 7	
OUTPUT FORMAT-H									
	0/8	***1/***9	***2/***A	***3/***B	***4/***C	***5/***D	***6/***E	***7/***F	
00B*	0005 0006	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007	
00C*	0005 0006	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007	
00D*	0006 0006	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007	
00E*	0006 0006	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007	
00F*	0006 0006	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007	

// XEQ NOISY

RATE 1/2 THRESHOLD=0.500 EBNQ= 3.000

INTERVAL PROBABILITIES ARE

P(111)=0.001792
P(110)=0.006125
P(101)=0.019982
P(100)=0.050992
P(000)=0.101846
P(001)=0.159229
P(010)=0.194875
P(011)=0.465151

	111	110	101	100	000	001	010	011
129-	0	0	1	3	6	10	12	0
64-	0	0	0	0	0	0	0	32
32-	0	1	1	0	1	0	1	28
16-	0	1	0	1	1	0	1	28
8-	1	0	0	1	1	1	0	28
4-	1	0	0	1	1	1	0	28
2-	1	1	1	1	0	1	0	27
1-	0	0	1	1	0	1	0	29

ACTUAL PROBABILITIES ARE

P(111)=0.001708
P(110)=0.006103
P(101)=0.020019
P(100)=0.051025
P(000)=0.101806
P(001)=0.159301
P(010)=0.194824
P(011)=0.465209

PERCENTAGE ERROR

-4.66%
-0.40%
0.15%
0.06%
-0.03%
0.04%
-0.02%
0.01%

ORIGINAL PAGE IS
OF POOR QUALITY

LMC4-3.0 D9		NOISE ROM 3.0 D9		82S129		(VXXXXX) J08-		PAGE 1	
OUTPUT FORMAT-H		***0/***8	***1/***9	***2/***A	***3/***B	***4/***C	***5/***D	***6/***E	***7/***F
000*	0001 0000	0007 0007	0002 0001	0002 0000	0003 0000	0003 0000	0003 0002	0001 0000	
001*	0000 0000	0007 0007	0004 0006	0004 0006	0004 0005	0004 0005	0001 0000	0005 0007	
002*	0004 0004	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007	0005 0007	0007 0007	
003*	0004 0004	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007	
004*	0004 0004	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007	
005*	0005 0005	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007	
006*	0005 0005	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007	
007*	0005 0005	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007	
008*	0005 0005	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007	
009*	0005 0005	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007	
00A*	0006 0006	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007	

ORIGINAL PAGE IS
OF POOR QUALITY

LMCV-3.0 DB		NOISE ROM 3.0 DB		M2S129		(XXXXXX)		JOB-		PAGE	
OUTPUT FORMAT-H											
	0/8	***1/***9	***2/***A	***3/***B	***4/***C	***5/***D	***6/***E	***7/***F			
00B*	0006 0006	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007		
00C*	0006 0006	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007		
00D*	0006 0006	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007		
00E*	0006 0006	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007		
00F*	0006 0006	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007		

// XEQ NOISY

RATE 1/2 THRESHOLD=0.500 EBNO= 4.000

INTERVAL PROBABILITIES ARE

P(111)=0.001018
P(110)=0.003852
P(101)=0.013668
P(100)=0.037955
P(000)=0.082489
P(001)=0.140325
P(010)=0.186863
P(011)=0.533827

	111	110	101	100	000	001	010	011
129-	0	0	0	2	5	8	11	6
64-	0	0	1	0	0	1	1	29
32-	0	0	1	1	0	1	1	28
16-	0	1	1	1	1	1	0	27
8-	1	1	0	0	1	0	1	28
4-	0	1	0	1	1	1	1	27
2-	0	1	0	0	1	1	1	28
1-	0	1	0	1	1	0	1	28

ACTUAL PROBABILITIES ARE

P(111)=0.000976
P(110)=0.003784
P(101)=0.013671
P(100)=0.037963
P(000)=0.082519
P(001)=0.140360
P(010)=0.186757
P(011)=0.533935

PERCENTAGE ERROR

-4.08%
-1.76%
0.02%
0.02%
0.03%
0.03%
-0.05%
0.02%

ORIGINAL PAGE IS
OF POOR QUALITY

LMC4-4.0 DB		NOISE ROM 4.0 DB		82S129		(XXXXXX)		JOB-		PAGE
OUTPUT FORMAT-H										
	0/8	***1/***9	***2/***A	***3/***B	***4/***C	***5/***D	***6/***E	***7/***F		
000*	0000 0000	0001 0005	0001 0000	0002 0001	0003 0002	0002 0000	0002 0004	0002 0007		
001*	0004 0004	0006 0007	0005 0006	0000 0004	0004 0006	0004 0005	0005 0006	0004 0006		
002*	0004 0004	0007 0007	0007 0007	0005 0007	0007 0007	0006 0007	0007 0007	0007 0007		
003*	0004 0005	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007		
004*	0005 0005	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007		
005*	0005 0005	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007		
006*	0005 0005	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007		
007*	0005 0006	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007		
008*	0006 0006	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007		
009*	0006 0006	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007		
00A*	0006 0006	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007		

ORIGINAL PAGE IS
OF POOR QUALITY

LMCN-4.0 DB		NOISE ROM 4.0 DB		825129		(XXXXXX) JOB-		PAGE 2	
OUTPUT FORMAT-H		***0/***8	***1/***9	***2/***A	***3/***B	***4/***C	***5/***D	***6/***E	***7/***F
00B*	0006 0006	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007
00C*	0006 0006	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007
00D*	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007
00E*	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007
00F*	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007

// XEQ NOISY

RATE 1/2 THRESHOLD=0.500 E9N0= 5.000

INTERVAL PROBABILITIES ARE

P(111)=0.000522
P(110)=0.002210
P(101)=0.008622
P(100)=0.026323
P(000)=0.062896
P(001)=0.117626
P(010)=0.172196
P(011)=0.609601

	111	110	101	100	000	001	010	011
129-	0	0	0	1	3	7	10	11
64-	0	0	1	1	2	0	1	27
32-	0	0	0	0	0	1	1	30
16-	0	1	0	1	0	1	1	28
8-	0	0	0	0	0	1	1	30
4-	1	0	1	1	0	1	0	28
2-	0	1	1	1	0	0	0	29
1-	0	0	1	0	0	1	1	29

ACTUAL PROBABILITIES ARE

P(111)=0.000483
P(110)=0.002197
P(101)=0.008666
P(100)=0.026245
P(000)=0.062866
P(001)=0.117675
P(010)=0.172241
P(011)=0.609619

PERCENTAGE ERROR

-6.50%
-0.56%
0.51%
-0.29%
-0.04%
0.04%
0.02%
0.00%

ORIGINAL PAGE IS
OF POOR QUALITY

LMCN-5.0 DB		NOISE ROM 5.0 DB		R2S129		(XXXXXX)		JOB-	PAGE
OUTPUT FORMAT-H		***U/***8	***1/***9	***2/***A	***3/***B	***4/***C	***5/***D	***6/***E	***7/***F
000*	0000 0004	0001 0000	0005 0006	0002 0000	0005 0006	0003 0001	0002 0001	0001 0005	
001*	0004 0004	0004 0004	0007 0007	0005 0006	0007 0007	0000 0005	0000 0007	0006 0007	
002*	0005 0005	0006 0007	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007	
003*	0005 0005	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007	
004*	0005 0005	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007	
005*	0005 0006	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007	
006*	0006 0006	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007	
007*	0006 0006	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007	
008*	0006 0006	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007	
009*	0006 0006	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007	
00A*	0006 0007	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007	

ORIGINAL PAGE IS
OF POOR QUALITY

LMCH-5.0 DB NOISE ROM 5.0 DB 925129 (XXXXXX) JCH- PAGE 2
OUTPUT FORMAT-H

	0/8	***1/***9	***2/***A	***3/***B	***4/***C	***5/***D	***6/***E	***7/***F
00B*	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007
00C*	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007
00D*	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007
00E*	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007
00F*	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007

// XEQ NOISY

RATE 1/2 THRESHOLD=0.500 EBNQ= 5.500

INTERVAL PROBABILITIES ARE

P(111)=0.000357
P(110)=0.001607
P(101)=0.006605
P(100)=0.021235
P(000)=0.053426
P(001)=0.105209
P(010)=0.162176
P(011)=0.649380

	111	110	101	100	000	001	010	011
129-	0	0	0	1	3	6	10	12
64-	0	0	0	0	0	1	0	31
32-	0	0	1	1	1	0	1	28
16-	0	0	1	0	1	1	0	29
8-	0	1	0	1	0	1	0	29
4-	0	1	1	1	0	0	1	28
2-	1	1	1	0	1	0	1	27
1-	0	0	0	1	0	0	1	30

ACTUAL PROBABILITIES ARE

P(111)=0.000244
P(110)=0.001708
P(101)=0.006591
P(100)=0.021240
P(000)=0.053344
P(001)=0.105224
P(010)=0.162231
P(011)=0.649414

PERCENTAGE ERROR

-31.74%
6.28%
-0.26%
0.02%
-0.15%
0.01%
0.03%
0.00%

ORIGINAL PAGE IS
OF POOR QUALITY

LMCN-5.5 DB		NOISE ROM 5.5 DB		925129		(YXXXXX)		JLF-		PAGE	
OUTPUT FORMAT-H											
	G/8	***1/***9	***2/***A	***3/***B	***4/***C	***5/***D	***6/***E	***7/***F			
000*	0000 0004	0005 0007	0001 0000	0001 0004	0002 0000	0002 0001	0003 0002	0004 0003			
001*	0004 0004	0007 0007	0004 0006	0005 0007	0005 0007	0006 0006	0001 0004	0007 0007			
002*	0005 0005	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007	0006 0007	0007 0007			
003*	0005 0005	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007			
004*	0005 0005	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007			
005*	0006 0006	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007			
006*	0006 0006	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007			
007*	0006 0006	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007			
008*	0006 0006	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007			
009*	0006 0006	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007			
00A*	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007			

ORIGINAL PAGE IS
OF POOR QUALITY

MCN-5.5 DB		NOISE ROM 5.5 DB				R2S120		(XXXXXX)		JLR-		PAGE	
OUTPUT FORMAT-H													
	0/8	***1/***9	***2/***A	***3/***B	***4/***C	***5/***D	***6/***E	***7/***F					
004*	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007					
00C*	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007					
00D*	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007					
00E*	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007					
00F*	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007	0007 0007					